InnovateFPGA
2018
Grand Final

AS 031

BreXting: Brain Texting

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High-level Project Description

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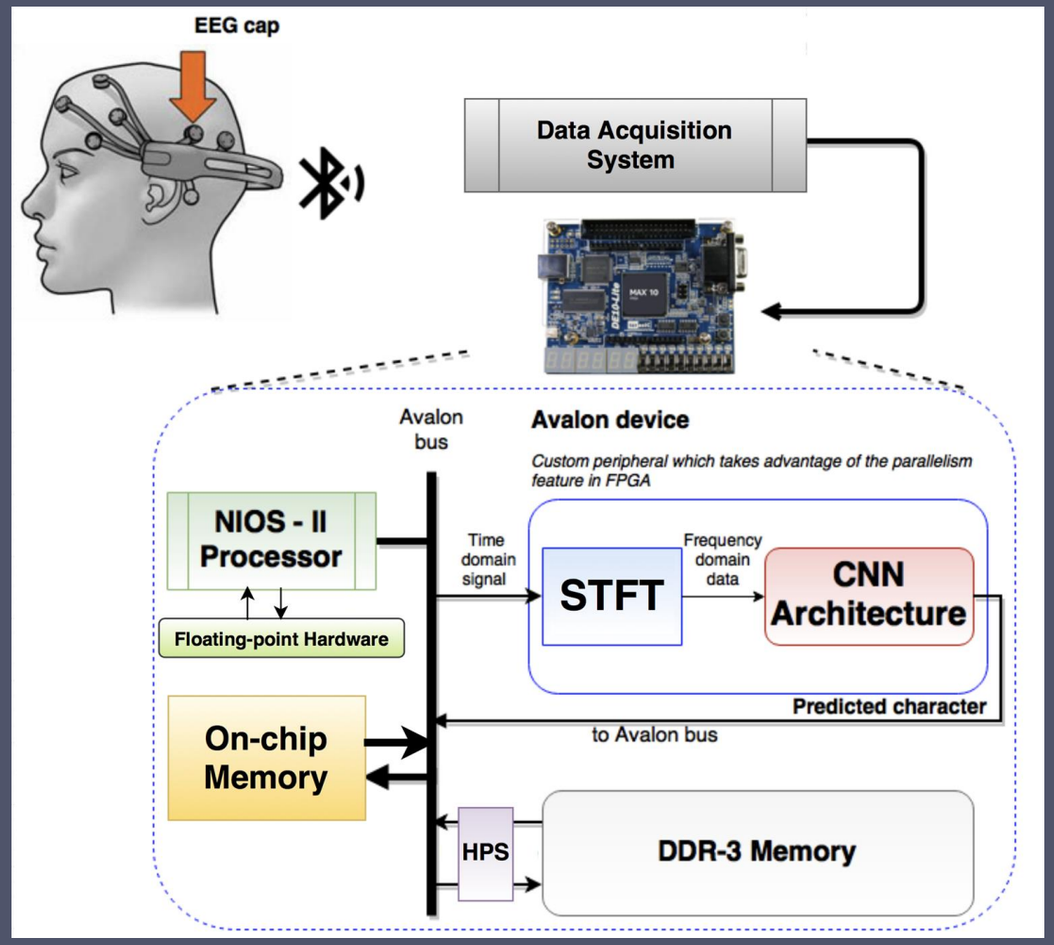
Our system involves three major blocks:

1) Recording EEG data to capture event related synchronization & desynchronization while the subject is thinking of respective motor tasks.

1) Conversion of time domain EEG to frequency domain to capture the relevant alpha & beta bands after noise removal and pre-processing.

1) Convolutional neural network implementation on FPGA using trained weights from subject's EEG data for four motor tasks. The network outputs triggers to move an on-screen pointer thus enabling to draw or type by thinking.



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Intel FPGA Virtues in Your Project

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- The Intel DE-10 Nano board contains various Hardware feature which will aid the development of this project.
- NIOS II – softcore processor which controls the overall flow of the system
- NIOS II Custom instructions for floating point computations
- High speed DDR3 SDRAM to store the data.

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Intel FPGA Virtues in Your Project

The main reasons for using an Embedded system for this project is to make the systems easily movable and real time. We use Intel FPGA because:

- Cyclone V SoC give an important advantage of Faster clock rates using the ARM processor and low power and targeted acceleration of the Intel Cyclone V FPGA.
- The tools provided by Intel such as Quartus, Qsys, Power Estimator allows fast development of the product.
- The IP Designs provided by Intel/Terasic, provide a great starting point to implement the designs.

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Functional Description

- The major contribution of the design is a basic framework for implementing a Deep learning-based Brain-Computer Interface (BCI) system on FPGA.

- Our primary goal was to move the mouse pointer using EEG signals from a subject. Once the subject is able to move the pointer, we plan to relay the output to a visual keyboard where the subject can control the pointer to type using the on-screen keyboard.

- Since the design is based on FPGA, it is supposed to be mobile and much more usable than current state-of-art machines.

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Functional Description

- For a proof of concept and to judge the potential of our design, we used one of the datasets from the BNCI Horizon 2020 database, specifically the 4-class motor imagery dataset
- A deep network is trained to classify each segment of EEG data into one of the 4 classes.
- With our current design, we can successfully classify the 4 classes with about 80% class-specific accuracy.

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Performance metrics

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The performance parameter for the application includes:

i) Development Time

ii) Number of decisions processed in 1 second

iii) Power consumed

iv) Area of the hardware on the design

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Current Results

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Area

- Logic Utilization : 6,286 / 41,910 (15%)
- Total Block Memory bit: 865,705 / 5,662,720 (15%)
- Total DSP block: 12/112 (11%)

Speed

- Latency : 6 ms/ per decision
- Clock frequency : 50 Mhz
- Max clock frequency : 80.44 Mhz
- Setup Time : 2.113 ns
- Hold Time : 0.083 ns

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Design Method

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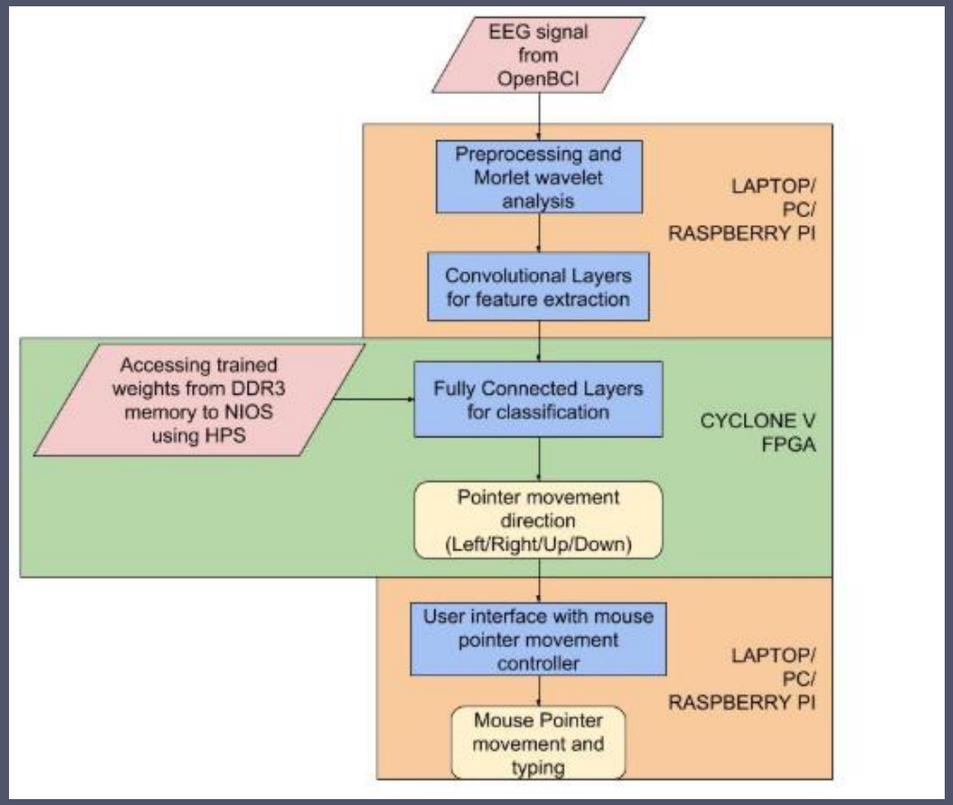
- Pre-processing to obtain EEG in Time-Frequency domain.
- Currently, the design architecture was trained on a GPU.
- The weights and parameters were obtained. These weights were converted into C arrays.
- The forward propagation of the convolutional neural network was implemented from scratch.



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Conclusion

Current Deliverables:

- Implementation of Fully Connected, Batch Normalization and Activation layers on FPGA using NIOS II softcore processor. Current design has 862 floating point parameters in the FPGA.
- DDR3 Memory access using HPS.
- Acceleration (14.3% reduction in time) using the In-built floating-point hardware module.
- Recognizing left, right, up, down movement direction from EEG signal to move the mouse pointer which selects the letters on on-screen keyboard.

Future Deliverables:

- The current system is not real time. The data is first preprocessed then loaded into the FPGA manually. Automating this process would be the next step.
- Replacing laptop/PC with Arduino/RaspberryPi to create a standalone system.