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2018
Grand Final

PR039

Memristive Neural Network

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Introduction

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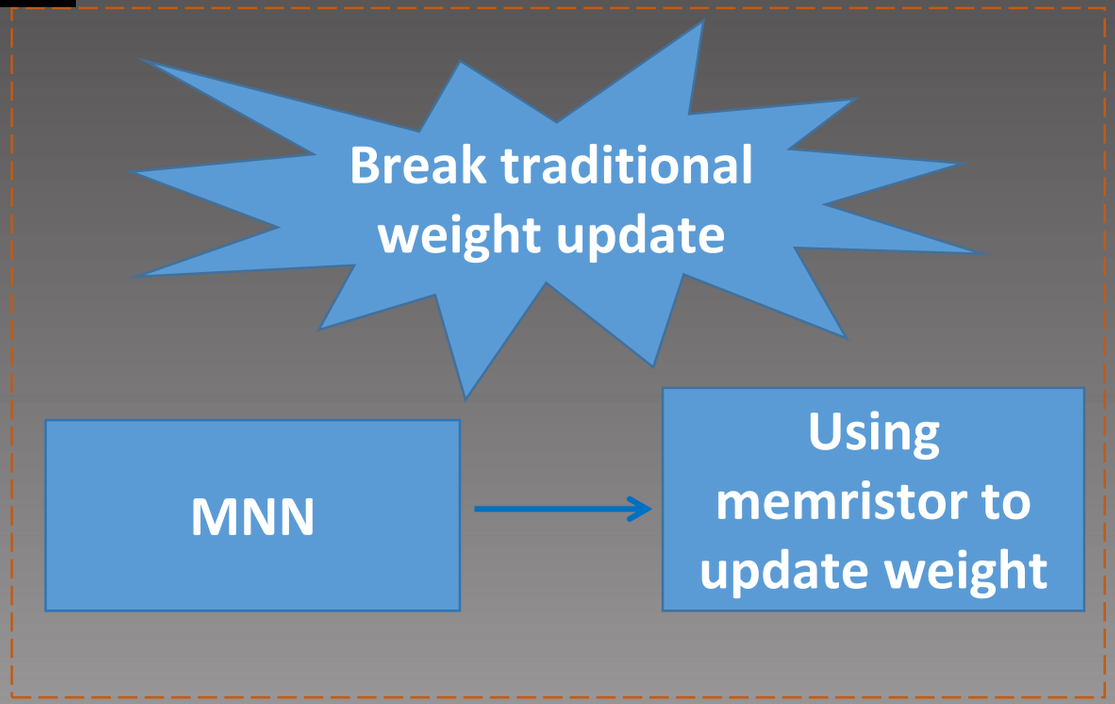
Memristive Neural Network



have large fluctuations in parameters

Digital integrated circuit implementation

Area

Speed

Weight sharing mechanism

Pipeline, clock constraints

Hardware friendly MNN

Design

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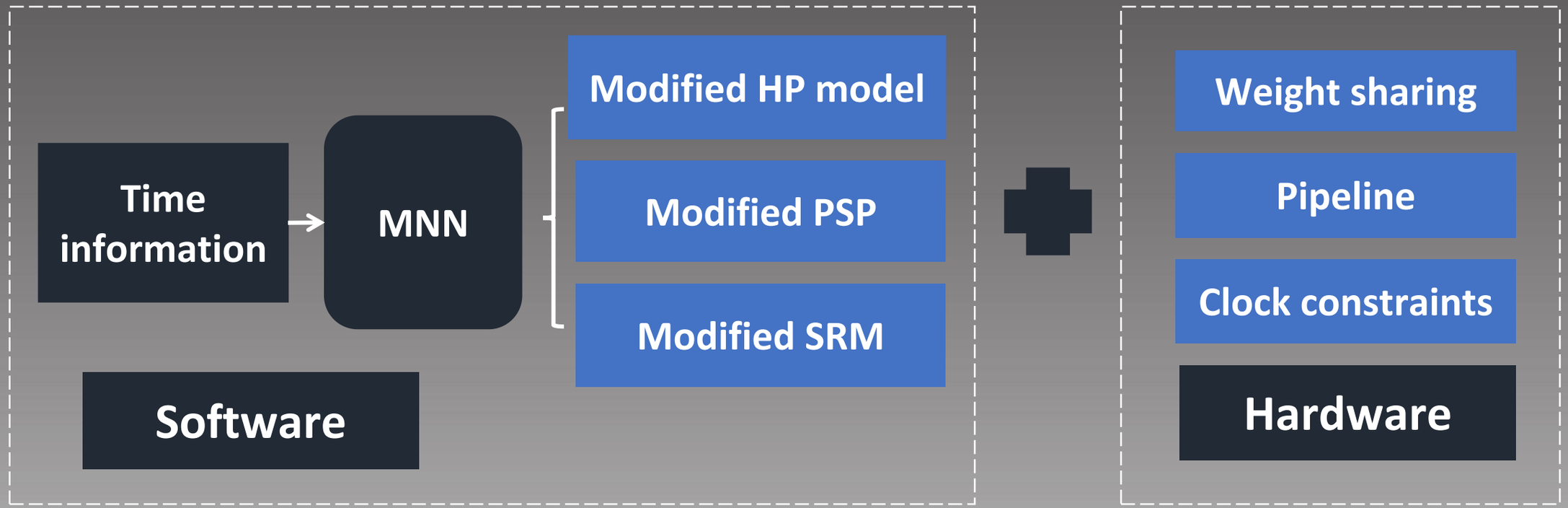
MNN Algorithm Design



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Modified HP Model

Traditional HP model

$$U(t) = \left[R_{off} - (R_{off} - R_{on})\mu_v \frac{R_{on}}{D^2}\int_{-\infty}^{t} I(t)dt\right] I(t)$$

Modified HP model

When I(t) is fixed to 1, the above formula is simplified as:

$$U(t) = \left[R_{off} - (R_{off} - R_{on})\mu_v \frac{R_{on}}{D^2}\int_{-\infty}^{t} dt\right] = k_1 - k_2\Delta t$$

So we can get:

$$M(t) = \frac{U(t)}{I(t)} = k_1 - k_2\Delta t$$

The memristor has a linear relationship with the time

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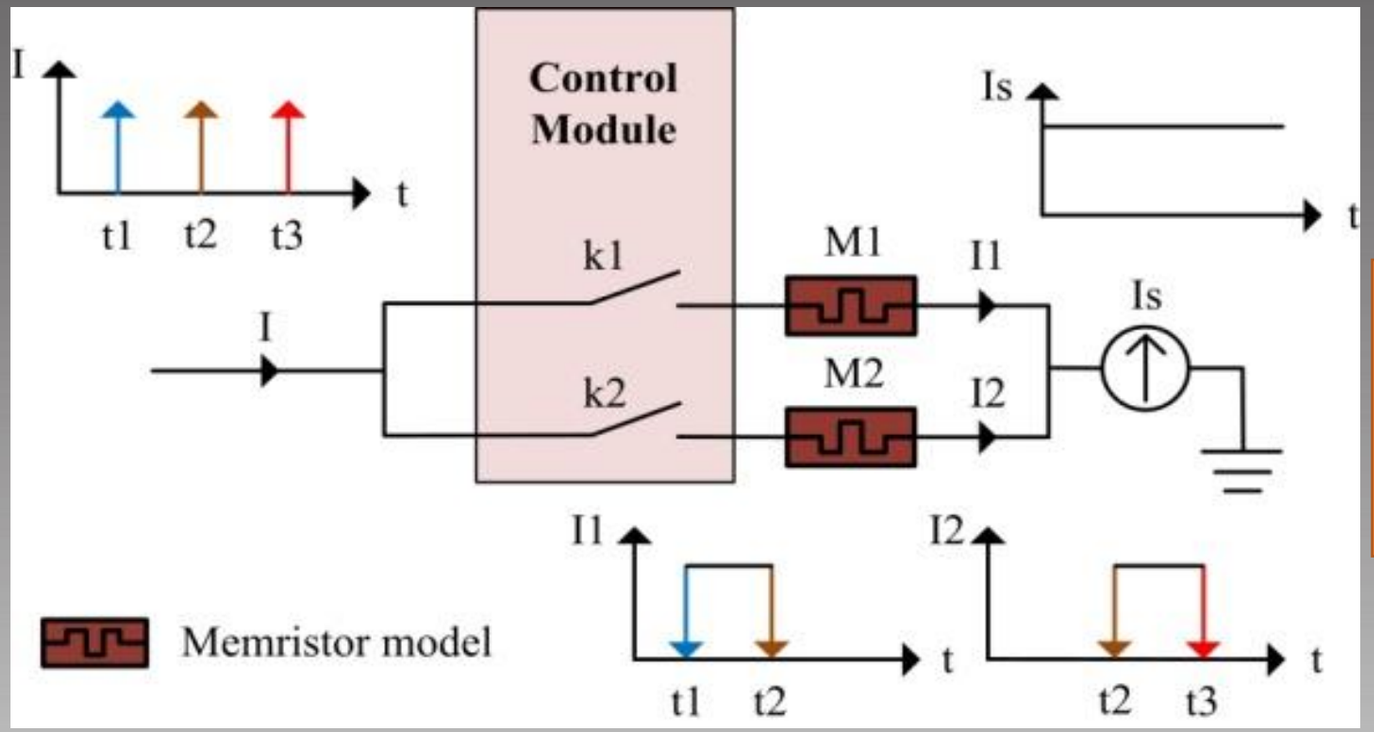
Modified HP Model

Modified HP model

$$M(t) = \frac{U(t)}{I(t)} = k_1 - k_2 \Delta t$$



Memristor-time module

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Design

Unsupervised Spike Response Model

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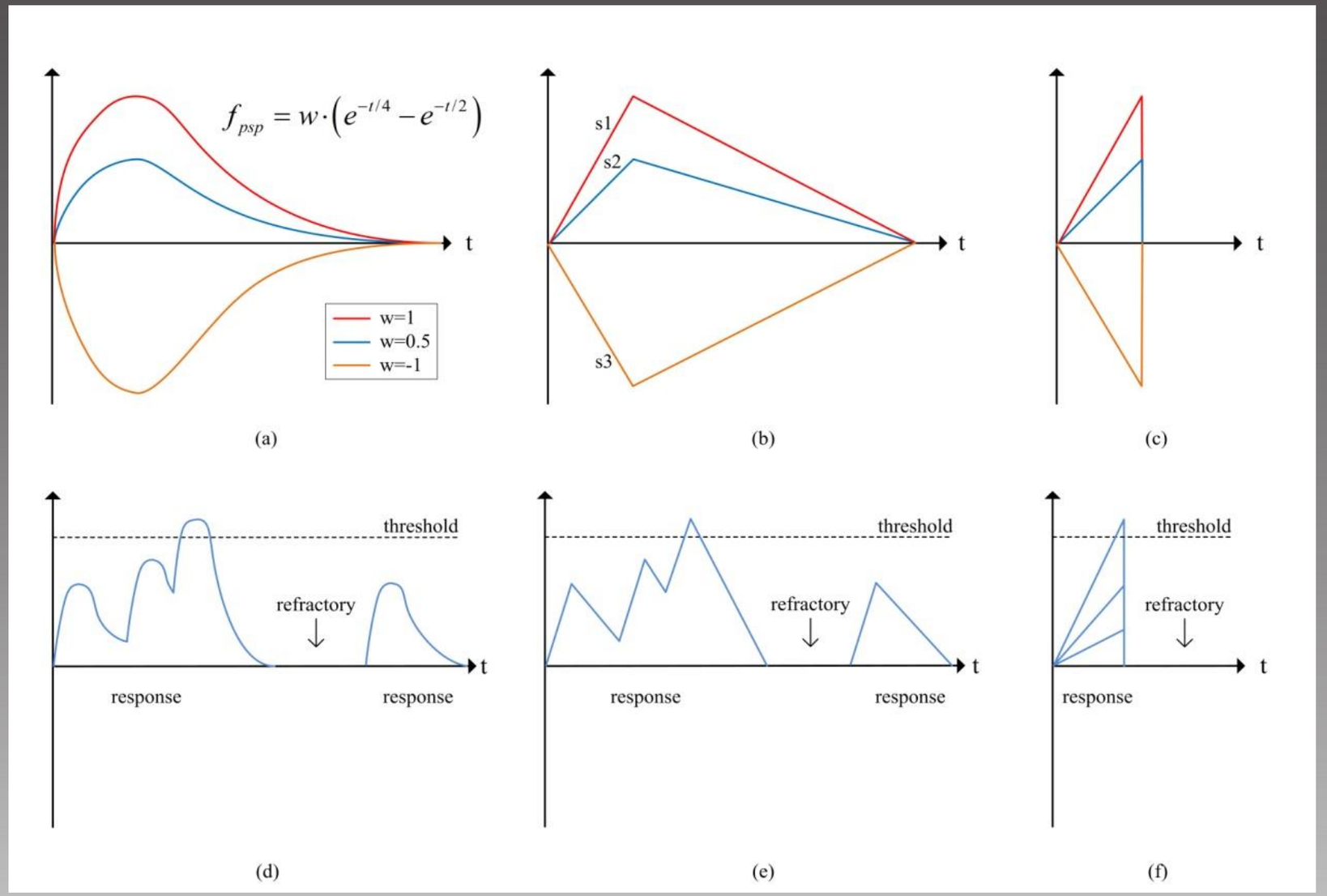
- PSP(Post synaptic potential)
- SRM(Spike response model)

Simplify for hardware implement



Design

Unsupervised Spike Response Model

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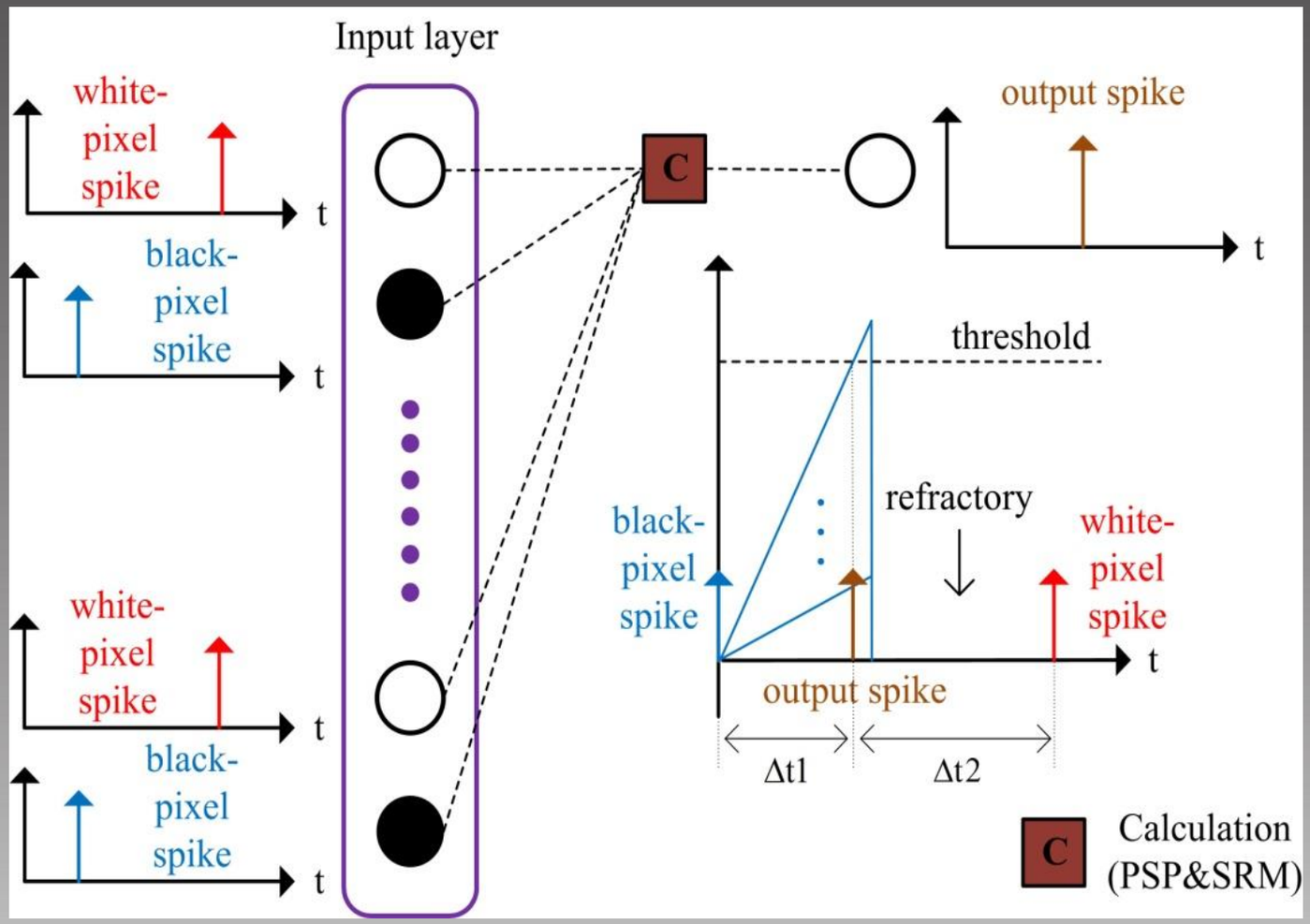
- **Learning process**



STDP!!!

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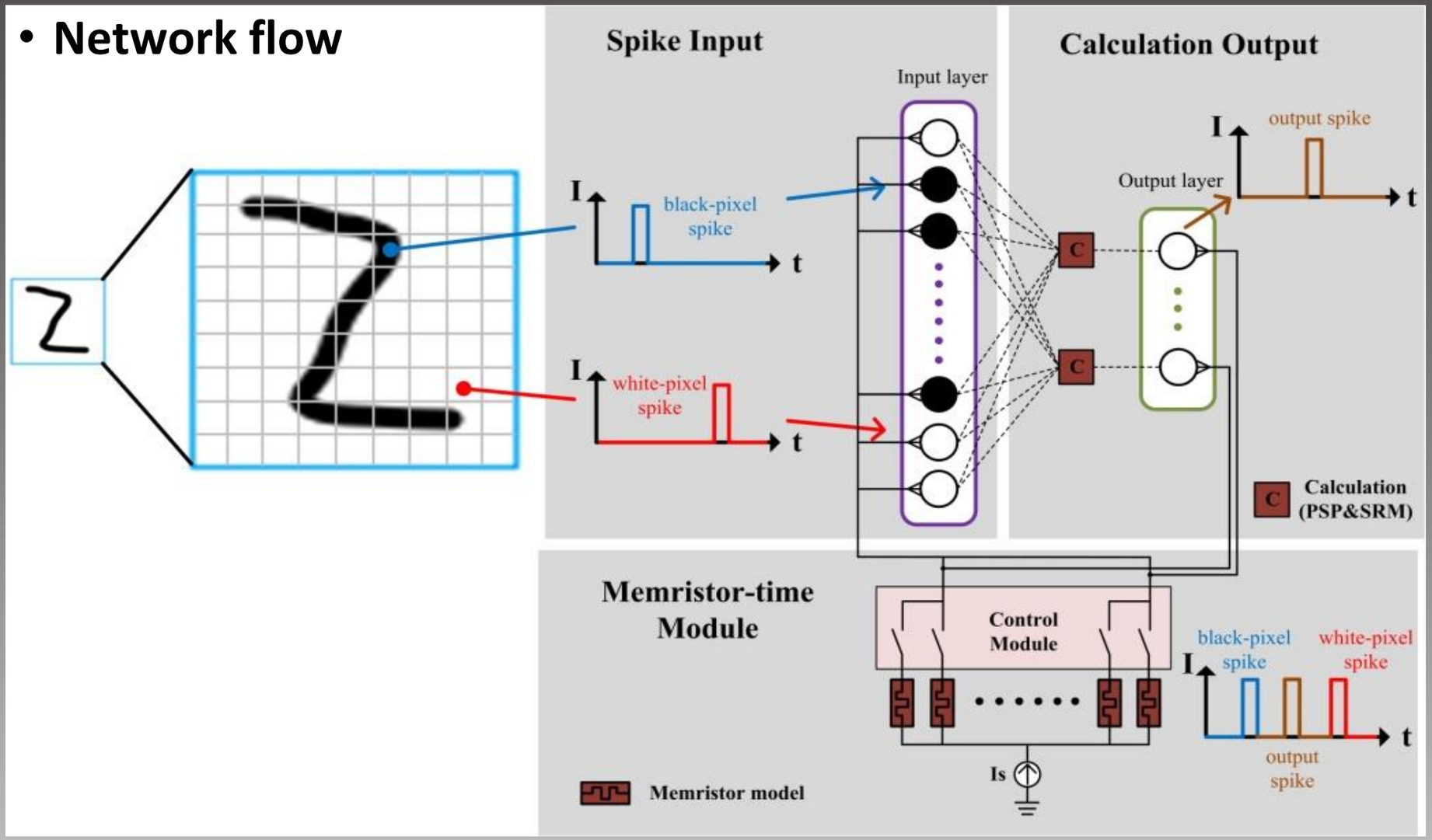
Design

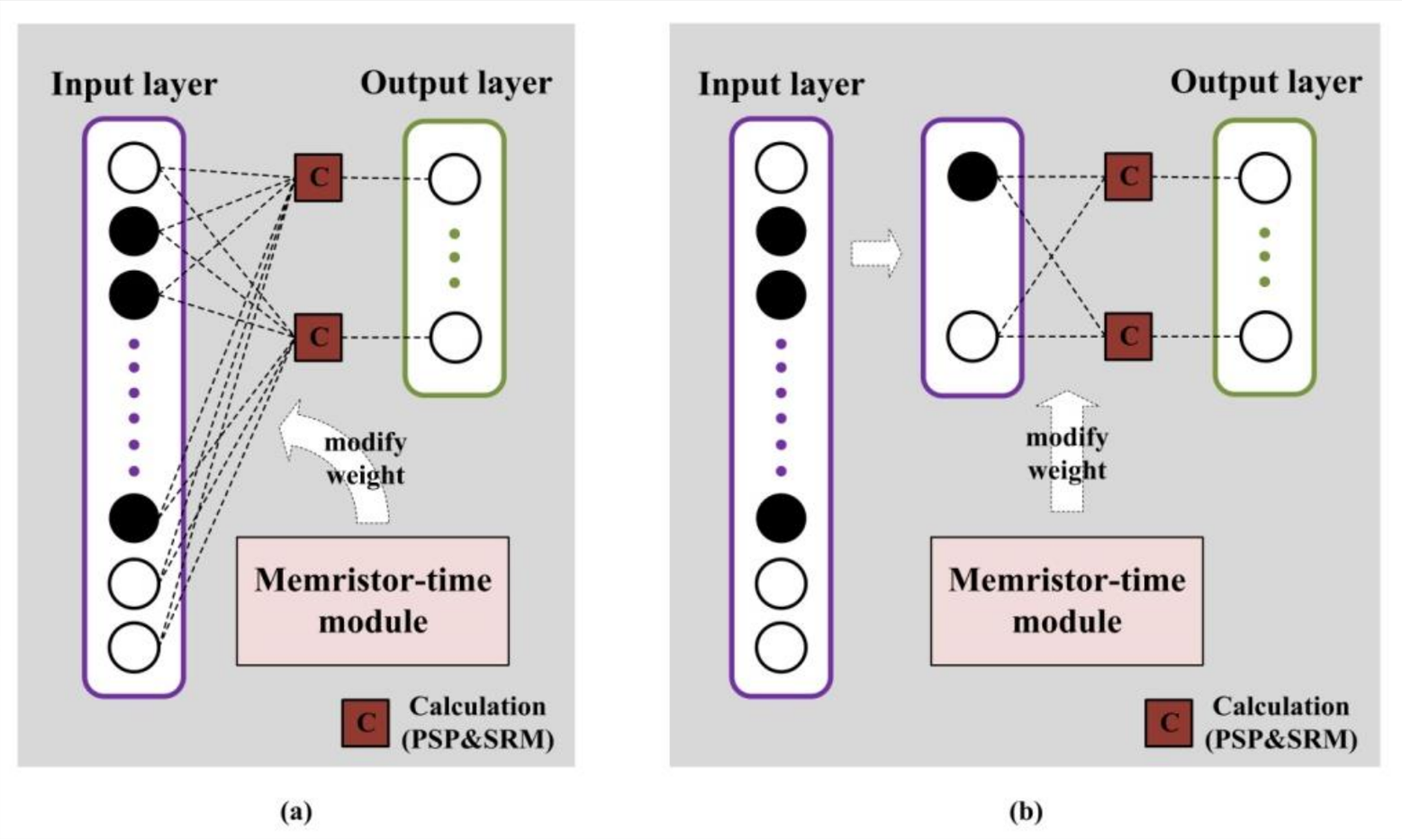
Hardware Architecture of MNN

- **Network flow**



Hardware Architecture of MNN

- **Weight sharing mechanism**



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Hardware Architecture of MNN

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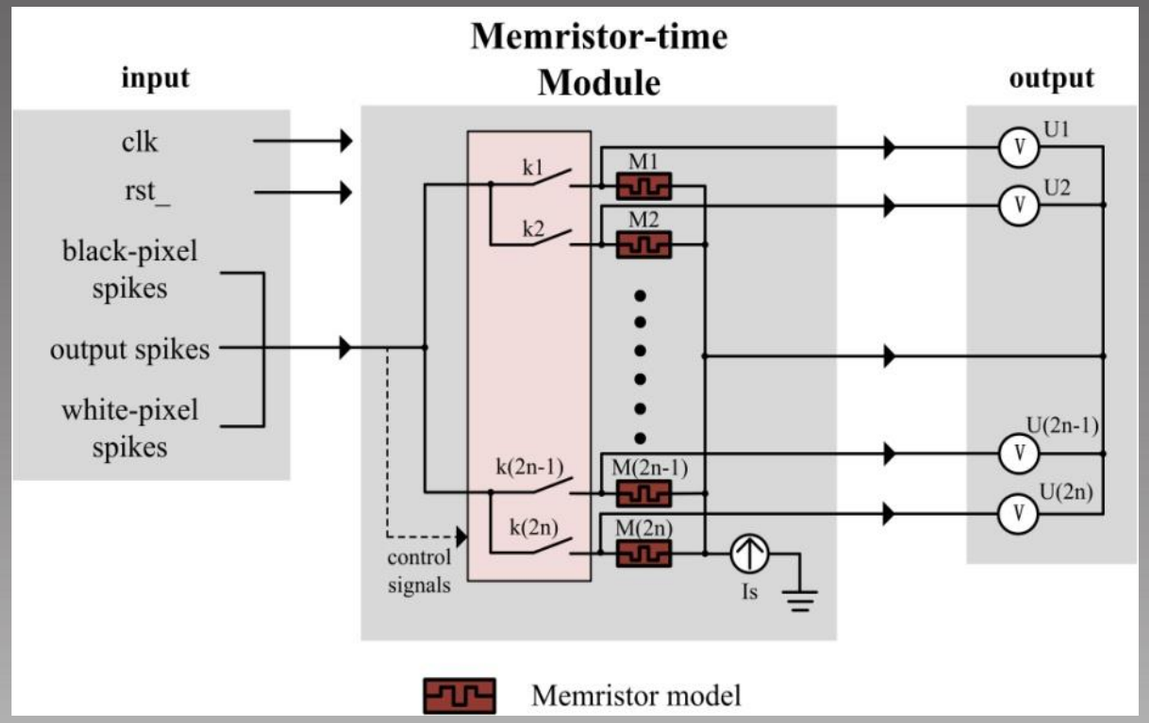
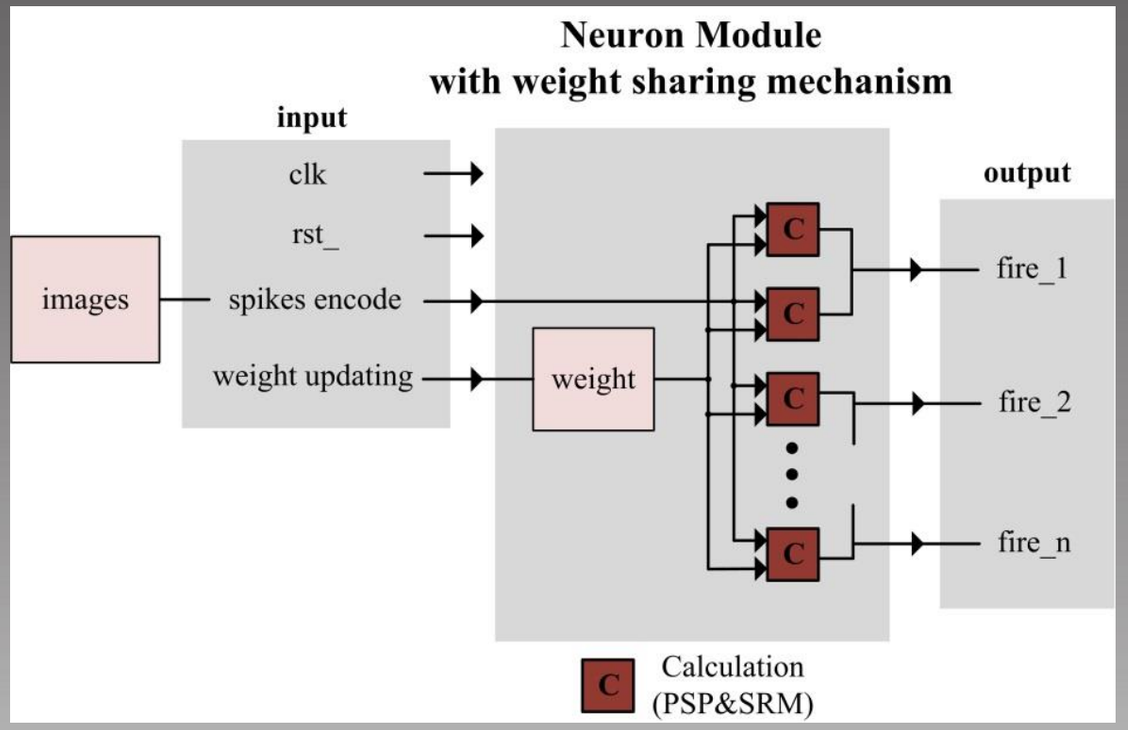
Circuit diagram of memristor-time module



Circuit diagram of neuron module with weight sharing mechanism



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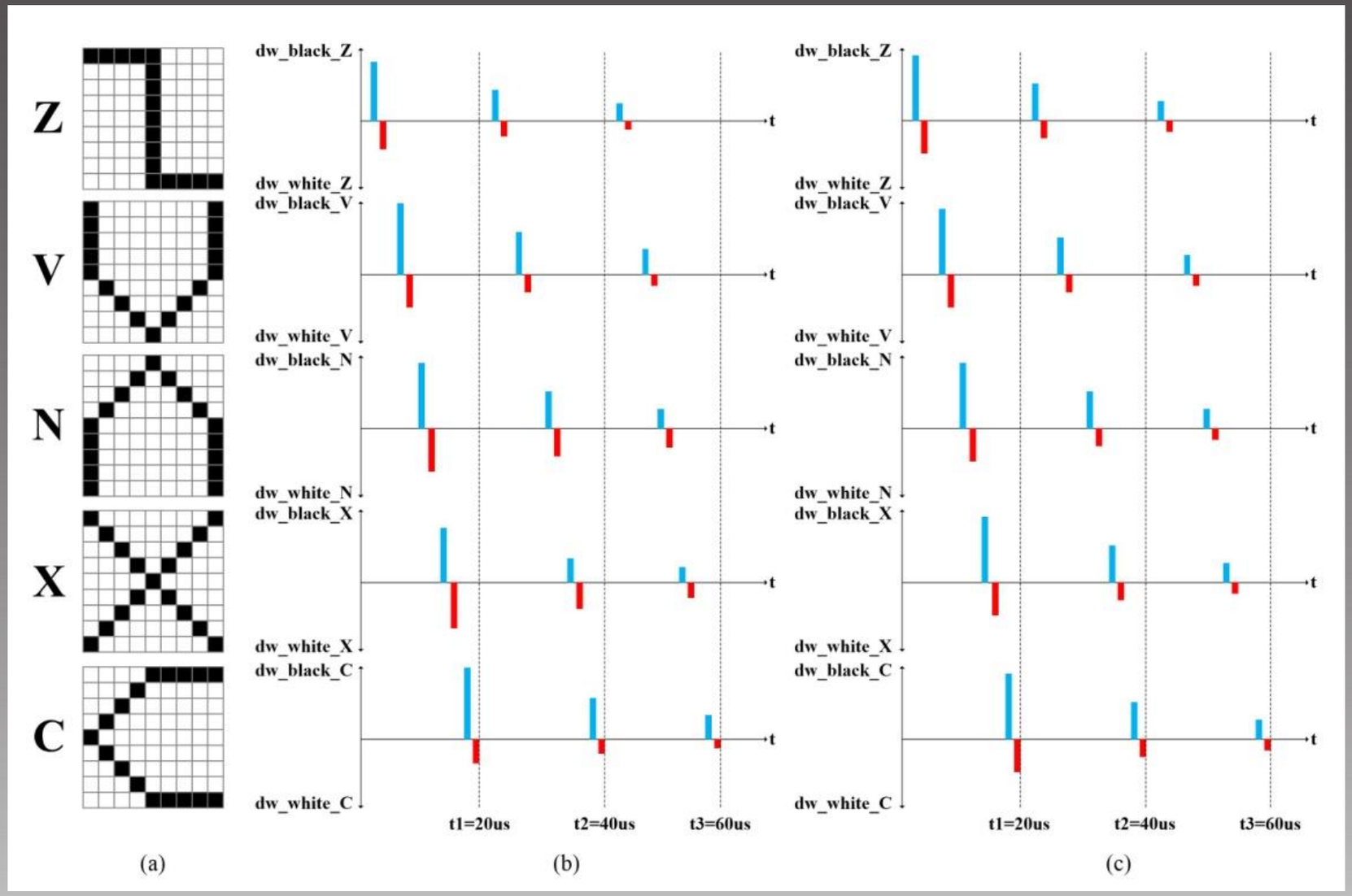
Test

Pattern Recognition Results



(a)The 9*9*5 network training images.

(b) The change of memristor's value in training process without weight share mechanism.

(c) The change of memristor's value in training process with weight share mechanism.

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Test

Pattern Recognition Results

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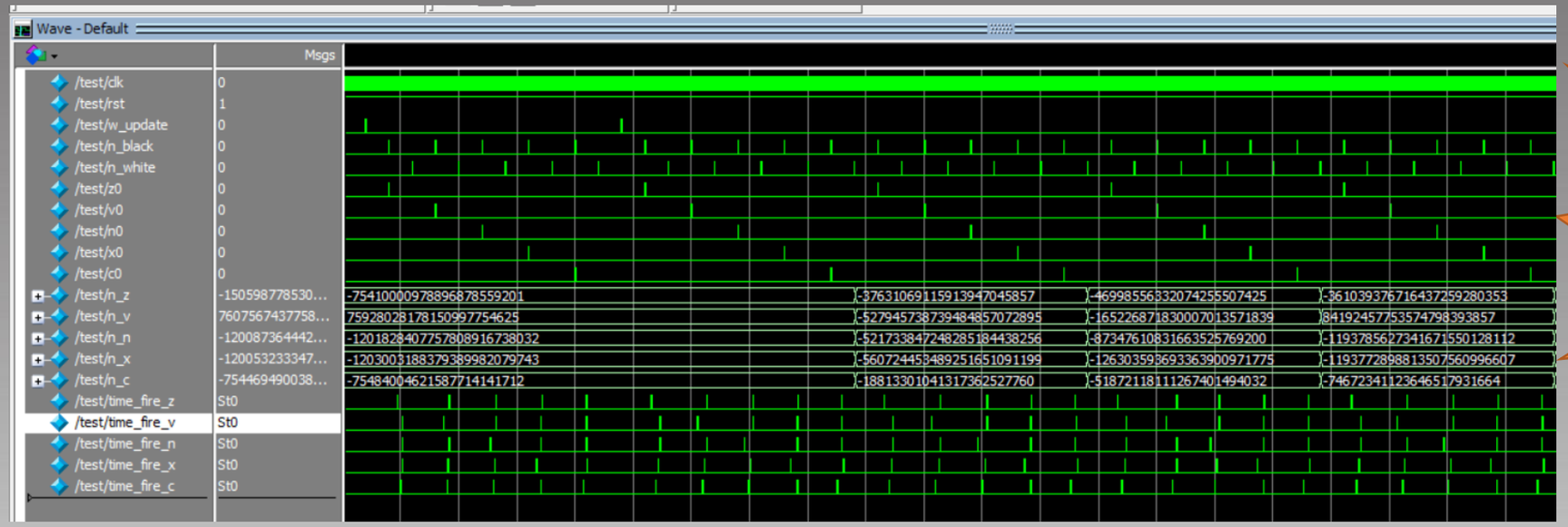
Random noise are added to each types of standard images and having 150 sets of images- total of 750 images

		Expectation				
		Z	**V**	**N**	**X**	**C**
Experiment results	**Z**	149	0	0	1	0
	V	0	149	0	0	1
	N	1	0	148	0	1
	X	0	1	0	149	0
	C	0	1	1	0	148



The accuracy is above 99%

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Resource Occupancy

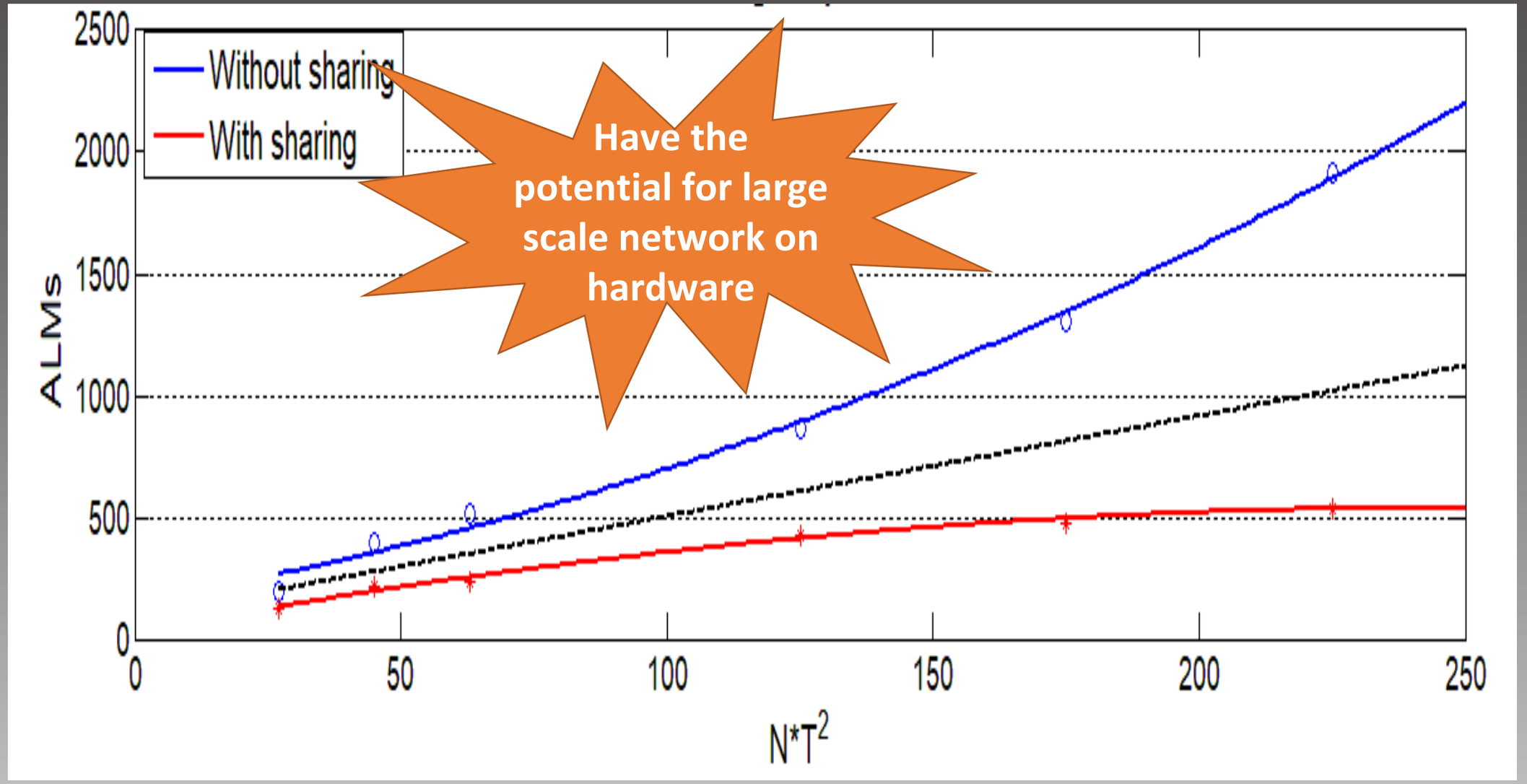
Resource occupancies of different scale networks on Stratix V

Network scale	Without weight sharing (in ALMs)	With weight sharing (in ALMs)
3*3*3	199	**122**
5*5*3	395	**214**
7*7*3	516	**237**
5*5*5	869	**428**
7*7*5	1309	**475**
9*9*5	1917	**540**

Resource occupancies of a 3*3*3 network on different hardware platforms

Hardware platforms	Without weight sharing	With weight sharing
Stratix V(in ALMs)	199	**122**
Cyclone 10(Total LE)	542	**477**
Arria 10(in ALMs)	203	**130**

Resource Occupancy



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Processing Speed

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Maximum clock frequency without weight sharing mechanism

Fmax (MHz)	Stratix V	Cyclone 10	Arria 10
9*9*5	247.52	128.3	235.02
7*7*5	243.07	125.06	226.55
5*5*5	256.54	126.5	227.32
7*7*3	248.51	126.21	242.01
5*5*3	250.69	125.42	237.25
3*3*3	270.12	126.29	246.67

Maximum clock frequency with weight sharing mechanism

Fmax (MHz)	Stratix V	Cyclone 10	Arria 10
9*9*5	249.88	140.11	248.76
7*7*5	258.93	137.78	245.16
5*5*5	267.52	138.5	240.21
7*7*3	242.84	137.87	244.74
5*5*3	258.2	136.87	246.37
3*3*3	250.25	138.08	244.98

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Performance Comparison

Design	Original model[24] (two-compartment)	Modified model[24] (two-compartment)	Our method	Our method
Platform	Cyclone IV: EP4CE115	Cyclone IV: EP4CE115	**Cyclone IV: EP4CE115**	**Stratix V: 5SGXEA7N2F45**
Recourse	3250 (LE)	3031 (LE)	**135 (LE)**	**70 (in ALMs)**
Mem-bits	122880	0	**0**	**0**
Multiplier	288	0	**0**	**0**
PLLs	0	0	**0**	**0**
Fmax	17.66MHz	40.68MHz	**86.21MHz**	**181.16MHz**

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Summary

1. Design modified HP model which can convert the time information into the value of memristor
2. Simplify PSP and SRM model for hardware implement
3. A weight sharing mechanism is designed
4. The processing speed is optimized by pipeline and clock constraints

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Thanks!